Amendments to the Specification

Paragraphs 0007 and 0008 on pages 2 and 3 have been amended to read as follows:

[0007] The present invention addresses these needs by providing a method of forming a memory device having a self-aligned contact. The memory device can provide an improved gate coupling ratio, photo window of contact, and cell planarization. In one embodiment, a method of forming a memory device having a self-aligned contact is provided which includes providing a substrate having a floating gate dielectric layer formed thereon, forming a floating poly gate layer on the floating gate dielectric layer, forming a first silicon nitride layer on the floating poly gate layer, and forming a patterned photoresist layer on the first silicon nitride layer. The method further includes etching exposed areas of the first silicon nitride layer and the floating poly gate layer using the patterned photoresist layer as an etch mask, forming an oxide layer over the exposed etched areas, removing the patterned photoresist layer and the first silicon nitride layer to expose the floating poly gate layer, forming poly spaces in the floating poly gate layer, and depositing a second silicon nitride layer over the poly spaces of the floating poly gate layer to form a self-aligned contact. The method can further comprise etching the second silicon nitride layer to create silicon nitride spacer formations, followed by depositing a second floating poly gate, forming an interlayer dielectric film (e.g., an oxide/nitride/oxide film) over the second floating poly gate, and then forming a control poly gate over the interlayer dielectric film.

[0008] In another embodiment, a method of forming a memory device having a self-aligned contact, comprises providing a substrate having a floating poly gate ~~feature~~layer and oxide features on source and drain sides of the floating poly gate ~~feature~~layer; forming poly spaces in the floating poly gate layer; and depositing a silicon nitride layer over the poly spaces of the floating poly gate ~~feature~~layer to form a self-aligned contact. The silicon nitride layer can be deposited over the floating poly gate ~~feature~~layer and the oxide features, and the method can further comprise etching the silicon nitride layer to expose a portion of the floating poly gate layer. The silicon nitride layer can be etched into silicon nitride spacer formations. Furthermore, the etching of the silicon nitride layer can prevent the formation of a random single bit defect caused by drain/source oxide defect, and the silicon nitride spacer formations can eliminate the random single bit defect between an interface of the floating poly gate feature and the oxide

features. The method can further comprise depositing an extra floating poly gate layer over the floating poly gate ~~feature~~layer, the oxide features, and the silicon nitride spacer formations to increase gate coupling ratio; and depositing an interlayer dielectric (such as an oxide/nitride/oxide stack film) on the floating poly gate layer and then depositing a control poly gate to form a flash device. In accordance with another aspect, the etching of the first silicon nitride layer comprises a- dry etch process. In other embodiments, apparatuses formed using the above methods are provided.

In the Abstract, lines 2 to 11 on page 14 have been amended to read as follows:

A method of forming a memory device having a self-aligned contact is ~~disclosed~~ described. The method includes providing a substrate having a floating gate dielectric layer formed thereon, forming a floating poly gate layer on the floating gate dielectric layer, forming a first silicon nitride layer on the floating poly gate layer, and forming a patterned photoresist layer on the first silicon nitride layer. The method further includes etching the first silicon nitride layer and the floating poly gate layer using the patterned photoresist layer as an etch mask, forming an oxide layer over the exposed etched areas, removing the patterned photoresist layer and the first silicon nitride layer to expose the floating poly gate layer, forming poly spaces in the floating poly gate layer, and depositing a second silicon nitride layer over the poly spaces of the floating poly gate layer to form a self-aligned contact.